REMARKS

This paper is being provided in response to the Office Action mailed November 9, 2004, for the above-referenced application. In this response, Applicants have cancelled withdrawn claims 8-19 without prejudice or disclaimer of the subject matter thereof, amended claim 1, and added new claims 20-26 to clarify that which Applicants consider to be the invention. Applicants respectfully submit that the amendments to the claims and the new claims are supported by the originally-filed specification.

The objection to the drawings has been addressed by amendments contained herein, as explained above. Accordingly, Applicants respectfully request that this objection be reconsidered and withdrawn.

The rejection of claims 1-6 under 35 U.S.C. 102(e) as being anticipated by U.S. Published Patent Application No. 2004/0124532 to Harada (hereinafter "Harada '532") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

Independent claim 1, as amended herein, recites a semiconductor device. An interconnect layer is provided on a semiconductor substrate. A protective film is provided on the interconnect layer. An electrode pad is provided on the protective film. An anti-oxidizing layer containing a different element which is different from an element contained in the interconnect layer is disposed between the interconnect layer and the protective film. The electrode pad is in electrical contact with the interconnect layer and is disposed on said protective film in a position

to permit contact by a probe. The different element of the anti-oxidizing layer has a lower oxidation-reduction potential than that of the element contained in said interconnect layer and said anti-oxidizing layer is disposed on the interconnect layer to inhibit corrosion of the interconnect layer when an interface between the electrode pad and the interconnect layer is damaged by said probe. Claims 2-7 depend directly or indirectly on independent claim 1.

The Harada '532 reference discloses a semiconductor device and method of manufacture a layered semiconductor device formed in an interconnection channel 107 having a central region and a peripheral region. The interconnection channel is approximately 100 nm to 2000 nm in width. The central region is positioned in a through hole 106 that extends further into the semiconductor device than said peripheral region. A lower interconnect layer 102 is positioned at the bottom of the through hole and an upper interconnect layer 113 is in electrical contact with the lower interconnect layer via the through hole. The upper interconnect layer includes a Ti film 108 covering the inner sidewalls and bottom of the through hole and the interconnection channel; a TiN film 109 deposited on the Ti film 108; a silicon containing TiN (TiSiN) film 110 formed on the TiN film 109; a Cu film 111 deposited on the TiSiN film 110; and another Cu film 112 deposited on the Cu film 111. (See paragraphs 0091-0093 and Figure 7 of Harada '532.)

Applicants' independent claim 1, as amended herein, recites that in a semiconductor device, an electrode pad is in electrical contact with an interconnect layer and is disposed on a protective film in a position to permit contact by a probe, wherein an anti-oxidizing layer, containing a different element than an element of the interconnect layer and that has a lower oxidation-reduction potential than the element of the interconnect layer, is disposed on the

interconnect layer to inhibit corrosion of the interconnect layer when an interface between the electrode pad and the interconnect layer is damaged by said probe. Since the protective film is formed on the interconnect layer, better mechanical strength is obtainable, and the damage by impact of a probe that occurs when the electrode pad is poked with the probe during non-defective/defective screening can be inhibited. In addition, the oxidation of the interconnect metal is effectively inhibited by the action and configuration of the anti-oxidizing layer, even when a part of the interconnect layer is exposed by the contact of the probe. Since the semiconductor device as presently claimed has the anti-oxidizing layer between the interconnect layer and the protective film, even though the upper layer of the interconnect layer is damaged in the case of being poked with the probe and the surface of the interconnect layer is exposed, the different element in the anti-oxidizing layer, which is different from an element contained in the interconnect layer, is oxidized by containing the atmospheric air. Thus, the chemically stable layer that prevents the corrosion of copper is formed on the surface of the interconnect layer, and thereby inhibiting the deterioration of the semiconductor device. The present claimed invention prevents the corrosion of the interconnect layer in the case of being poked with the probe, by providing the synergistic effect of the protective film and the anti-oxidizing layer configured as claimed. (See page 6, lines 9 - page 7, line 4 of the present application.)

Applicants respectfully submits that Harada '532 does not teach or fairly suggest at least the above-noted features as claimed by Applicant. Specifically, Harada '532 discloses a semiconductor device having an interconnection channel 107 of approximately 100 nm to 2000 nm in width. Within the interconnection channel is a through hole 106 containing a plurality of layers positioned along the bottom and sides. The configuration and dimensions of the

interconnection channel disclosed by Harada '532 indicate that Harada '532 arguably does not disclose an electrode pad disposed on a protective layer that is electrically connected to an interconnect layer and that is disposed to receive a probe, wherein an anti-oxidizing layer is disposed on the interconnect layer and contains a different element from the element of the interconnect layer that inhibits corrosion of the interconnect layer when an interface is damaged between the electrode pad and the interconnect layer as a result of impact by the probe. The anti-oxidizing layer as claimed by Applicants inhibits corrosion of the interconnect layer, even if the interconnect layer is exposed by the damage resulting from the probe. As noted in Figure 7 of Harada '532 and by paragraph 0095, the structure of the semiconductor device, in which an upper interconnect layer 113 overlies the semiconductor device and is electrically connected to the lower interconnect layer 102 through holes 106, is designed to reduce leakage current flowing between the through holes 106 and between adjacent portions of the upper interconnect layer 113 and does not have the structure, as claimed by Applicants, to inhibit corrosion of an interconnect layer at an interface of the interconnect layer with an electrode pad when the interface is damaged by a probe impacting an electrode pad.

Accordingly, Applicant respectfully submits that Harada '532 does not teach or fairly suggest at least the above-noted features as claimed by Applicant. In view of the above, Applicants respectfully request that this rejection be reconsidered and withdrawn.

The rejection of claims 1-7 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,777,811 to Harada (hereinafter "Harada '811") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

The features of independent claim 1 are discussed above. Claims 2-7 depend therefrom.

The Harada '811 reference discloses a semiconductor device similar to that described above with respect to Harada '532. Further, the Office Action cites Harada '811 as disclosing an interconnect layer in which an upper portion of the layer is modified to comprise a different element than an element contained in the interconnect layer. (See Figure 7 and element 109 of Harada '811).

Applicants respectfully submit that Harada '811 does not teach or fairly suggest at least the features of a semiconductor device having an electrode pad is in electrical contact with an interconnect layer and is disposed on a protective film in a position to receive a probe, wherein an anti-oxidizing layer, containing a different element than an element of the interconnect layer and that has a lower oxidation-reduction potential than the element of the interconnect layer, is disposed on the interconnect layer as to inhibit corrosion of the interconnect layer when an interface between the electrode pad and the interconnect layer is damaged by the probe, as is claimed by Applicants. Like the discussion above of Harada '532, Harada '811 discloses a wiring groove 107 in which is embedded via holes 106 and which includes multiple layers having a structure that is designed to prevent leakage current that would result form a single layer structure design. (See col. 12, lines 18-35 of Harada '811.)

Applicants respectfully submit that new claims 20-26 are also patentable over the art of record.

Based on the above, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
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AMENDMENTS TO THE DRAWINGS:

Replacement Drawing Sheets 10 and 11 are attached hereto containing revised Figures 10A-11B. The legend "Prior Art" has been added to the revised figures as required in the Office Action. Applicants respectfully submit that no new matter is added by the amendments to the drawings.